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IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Hamm et al. Case: 12-14-9-7-5  
Serial No.: 09/433,204 Group Art Unit: 2245  
Filing Date: November 4, 1999 Examiner: T. Dang  
Title: A METHOD OF FABRICATING A HETEROJUNCTION  
BIPOLAR TRANSISTOR

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JAN 29 2003  
TECHNOLOGY CENTER 2800

THE COMMISSIONER OF PATENTS AND TRADEMARKS  
WASHINGTON, D.C. 20231

SIR:

AMENDMENT

In response to the Examiner Dang's Office Action dated November 6<sup>th</sup>, 2002,  
please enter the following response.

REMARKS

The Examiner's Office Action has been thoroughly considered. By way of the  
remarks herein, Applicant believes his application to be in condition for allowance.

In the instant Office Action, Examiner Dang has rejected independent Claim 16,  
and dependent Claims 17 and 19, under 35 U.S.C. § 102(b), as being anticipated by  
Yamahata, Japanese Patent 08-203435. Moreover, the Examiner has rejected dependent  
Claim 18 under 35 U.S.C. § 103, as being unpatentable over Yamahata, further in view  
of Costas et al., U.S. Patent Number 6,137,125 and dependent Claim 20 under 35 U.S.C.  
§ 103, as being unpatentable over Yamahata in view of Kasuya, Japanese Patent 08-  
017798.

I. Rejection of Claims 16, 17 and 19 Under 35 U.S.C. § 102(b)

Examiner Dang has rejected independent Claim 16, and dependent Claims 17  
and 19, as being anticipated by Yamahata, Japanese Patent 08-203435. Applicants

respectfully traverse the Examiner's anticipation rejection with respect to the art of record, including the Yamahata reference. Yamahata discloses a method of manufacturing a heterojunction bipolar transistor. The method of Yamhata includes spreading benzocyclobutene ("BCB") on the surface of a semiconductor device through spin coating and curing it to harden the BCB, thereby forming a passivation film 10. Passivation film 10 is apparently intended to protect the semiconductor device surface.

Applicants' believe that the Yamahata reference fails to teach or suggest the claimed invention. Applicants' Claim 16 recites the step of "forming a conductive post overlying the semiconductor region...." Applicants believe that the Yamahata reference neither teaches nor discloses forming a conductive post. Applicants believe that the Yamahata reference apparently shows the formation and curing of a passivation film (10) onto base, emitter and collector electrodes (7, 8 and 9). Apparently, a silicon oxide layer (11) and a photoresist layer (12) are respectively formed over the passivation film (10) in the Yamahata reference to support the formation of a hole (14). Thereafter, pad wiring (15) is formed through the hole (14) to access the emitter electrode (8), as shown for example, in FIG. 11 of the Yamahata reference.

Applicants advance that the Yamahata reference neither discloses nor suggest the formation of a conductive post. Applicants submit that a formed conductive post, as recited in Claim 16, is neither anticipated nor made apparent by the structure of the Yamahata reference, including pad wiring (15) formed after a hole (14) is formed in the passivation layer. In one merely exemplary embodiment of the present invention, Applicants teach forming a passivation layer 340 over formed conductive posts 320 and 330. As stated hereinabove, Applicants' Claim 16 recites the step of "forming a conductive post overlying ... a structure ...[and] encapsulating the structure...." Consequently, Applicants advance that Claim 1 defines novel and non-obvious matter.

Applicants further submit that dependent Claims 17 and 19 are also not anticipated by the art of record. These dependent claims depend from independent Claim 16, which is neither taught nor suggested by the Yamahata reference, as stated

hereinabove. Consequently, in view of the above remarks, Applicants submit that dependent Claims 17 and 19 also define novel and non-obvious matter.

## II. Rejection of Claim 18 Under 35 U.S.C. § 103

Examiner Dang has rejected dependent Claim 18 as being unpatentable over Yamahata, Japanese Patent 08-203435 in view of Costas et al., U.S. Patent Number 6,137,125. Applicants respectfully traverse the Examiner's obviousness rejection with respect to the art of record, including the Yamahata and Costas et al. references. Yamahata discloses a method of manufacturing a heterojunction bipolar transistor, as explained hereinabove. Costas et al. disclose a two-layer hermetic coating method for encapsulating GaAs monolithic microwave integrated circuits ("MMIC"). The Costas et al. reference discloses the use of benzocyclobutene ("BCB") to capacitively decouple the MMIC from a carrier substrate. As stated by Examiner Dang, Costas et al. further teaches curing BCB in a nitrogen atmosphere.

Applicants' submit that the Examiner's proposed combination fails to teach or suggest the claimed invention. More particularly, the formation of pad wiring through a hole to access an electrode of the Yamahata reference, when combined with the two-layer hermetic coating method for encapsulating GaAs MMIC of Costas et al., neither discloses nor suggests the step of "forming a conductive post overlying the semiconductor region," as recited in independent Claim 16. Consequently, the Yamahata and Costas et al. references, when taken individually or in combination, fail to teach and/or suggest the elements of dependent Claim 18.

## III. Rejection of Claim 20 Under 35 U.S.C. § 103

Examiner Dang has rejected dependent Claim 18 as being unpatentable over Yamahata, Japanese Patent 08-203435 in view of Kasuya, Japanese Patent 08-017798. Applicants respectfully traverse the Examiner's obviousness rejection with respect to the art of record, including the Yamahata and Kasuya references. Yamahata discloses a method of manufacturing a heterojunction bipolar transistor, as explained hereinabove.

The Kasuya reference discloses a dry etching processing method for a benzocyclobutene ("BCB") layer. More particularly, the Kasuya reference appears to teach the use of dry etching a BCB layer by supplying a gaseous mixture of CF<sub>4</sub> and O<sub>2</sub> or SF<sub>6</sub> and O<sub>2</sub>.

Applicants' submit that the Examiner's proposed combination fails to teach or suggest the claimed invention. More particularly, the formation of pad wiring through a hole to access an electrode of the Yamahata reference, when combined with the method for dry etching a BCB layer of Kasuya, neither discloses nor suggests the step of "forming a conductive post overlying the semiconductor region," as recited in independent Claim 16. Consequently, the Yamahata and Costas et al. references, when taken individually or in combination, fail to teach and/or suggest the elements of dependent Claim 20.

#### IV. Summary and Conclusion

Applicants believe that a full and complete response has been made to Examiner Dang's Office Action. Thus, in view of the hereinabove remarks, Applicants respectfully request reconsideration and allowance of their patent application and its claims. To that end, if the Examiner feels that a conference might expedite the prosecution of this case, he is cordially invited to call the undersigned.

Respectfully submitted,



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Date: January 21, 2003

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